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(54) Integrated inductive circuits

(57) An integrated inductive element (40a) may be formed over a substrate (42). A trench (80) may be defined in a variety of shapes in the substrate (42) beneath the integrated inductive element (40a) in order to reduce eddy current losses arising from magnetic coupling between integrated inductors associated with the same integrated circuit.

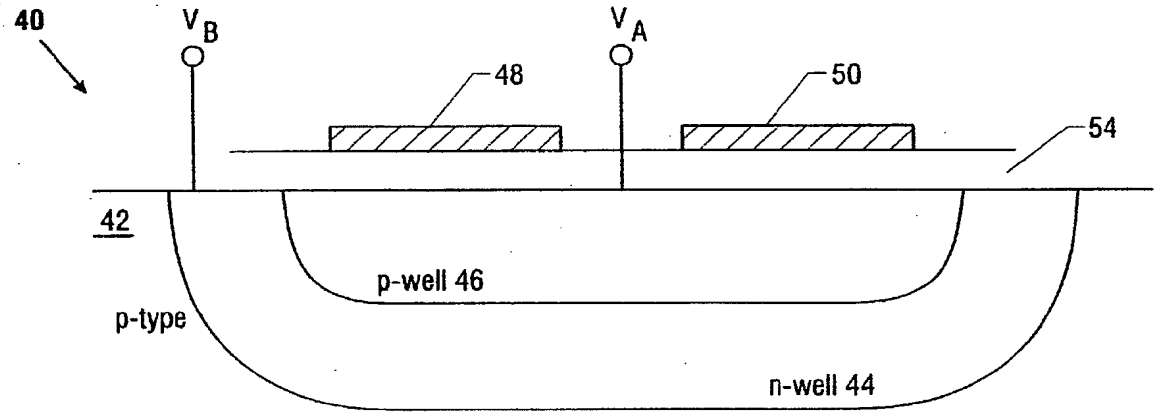

FIG. 4

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Description

Background

[0001] This invention relates generally to radio frequency (RF) integrated circuits that include active devices and passive components such as inductors and capacitors used for radio frequency devices such as cellular telephones and wireless network devices such as Bluetooth and other wireless devices and personal digital assistants.

[0002] The technology for manufacturing integrated circuits has conventionally divided integrated circuits into various categories based on the compatibility of processes and other considerations. Generally, radio frequency circuits have not been mixed with logic circuits in the same integrated circuit. Radio frequency circuits are analog circuits that are involved in filtering and detecting radio frequency signals such as cellular telephone signals. In contrast, logic circuits generally include transistors and other active components that form digital integrated circuit devices. Thus, for example, bipolar techniques may be utilized to manufacture radio frequency circuits and standard complementary metal oxide semiconductor (CMOS) processes may be utilized to manufacture logic circuits.

[0003] Memory circuits may account for still another category. Generally, special processes may be utilized in connection with the manufacture of memory circuits because of special design considerations such as multiple gate electrodes and special voltage supply needs. Thus, memory circuits are often fabricated separately from logic circuits.

[0004] Still another category are the so-called mixed signal circuits which may include both digital and analog components. These signals too may be accounted for separately so that a device that includes RF signal processing, RF integrated circuits, mixed signal circuits, logic circuits and memory circuits may be made up of a number of separately fabricated integrated circuit chips.

[0005] The cost of an electronic device may be closely correlated to the extent of integration that is possible. The more devices and the more types of devices that can be integrated into a single integrated circuit and manufactured using highly replicated techniques, the lower the resulting price. Unfortunately, because of incompatibilities between the different types of integrated circuits, it has not been possible, to date, to fabricate both radio frequency circuits, mixed signal circuits, logic circuits and memory circuits all on the same standard CMOS integrated circuit process.

[0006] One problem that arises in connection with radio frequency circuits in CMOS processes is that the passive components such as capacitors and inductors may be adversely affected by the substrates over which they are formed. In particular, coupling may occur between the substrate and integrated circuit inductors for example. This coupling may result in degraded performance of inductive circuits. As a result, inductive circuits may be formed in bipolar or silicon over insulator (SOI) integrated circuits rather than using standard CMOS logic processes. Thus, two or more integrated circuits are needed--one for logic, one for RF circuits, one for memory and one for mixed signals.

[0007] Some efforts have been made to overcome this coupling problem. For example, Silicon Wave Inc. has devised a so-called silicon over insulator (SOI) BiCMOS (Bipolar CMOS) integrated circuit which integrates both logic and radio frequency components onto the same die. However, the use of silicon over insulator technology greatly complicates the manufacturing process and increases cost. Moreover, the bulk of semiconductor fabrication facilities in the United States and the rest of the world are dedicated to manufacturing metal oxide semiconductor technologies. The SOI process is not amenable to widespread manufacturing at a number of highly expensive, already existent, fabrication facilities.

[0008] In addition to capacitive coupling of substrate noise, magnetic coupling between integrated inductors on the same integrated circuit may also be problematic. The coupling between integrated inductors on the same circuit may adversely effect the operation of any given inductor. For example, the magnetic coupling may change the operating parameters of one or more integrated inductors on the same integrated circuit.

[0009] The quality factor or Q factor strongly depends on the layout and the properties of the particular process technology. It is known that the quality of an integrated inductor may be adversely affected by the metal wire resistance, capacitive coupling to the substrate and magnetic coupling to the substrate. Capacitive and magnetic coupling limit the Q factor at relatively high frequencies. The magnetic coupling becomes more significant in CMOS technologies with doped substrates because the effect of substrate resistance appears in parallel with the inductor.

[0010] Thus, there is a substantial need to find a way to reduce coupling in integrated inductors.

Brief Description of the Drawings

[0011]

Figure 1 is a depiction of the various families of integrated circuit technologies that may be fabricated on the same integrated circuit in accordance with embodiments of the present invention;

Figure 2 is a block depiction of a cellular telephone in accordance with one embodiment of the present invention;

Figure 3 is a block diagram of a Bluetooth transceiver in accordance with one embodiment of the present invention;

Figure 4 is a greatly enlarged cross-sectional view of an inductive circuit element in accordance with

one embodiment of the present invention;
Figure 5 is a greatly enlarged top plan view of an inductive element in accordance with one embodiment of the present invention;
Figure 6 is an equivalent circuit of the inductive element shown in Figures 4 and 5;
Figure 7 is a perspective view of an embodiment of the inductive element shown in Figure 5;
Figures 8A and 8B are top plan views of two different layers of an inductive element that may be used in the present invention;
Figure 9 is an enlarged cross-sectional view of still another embodiment of an inductive element that may be utilized in connection with the present invention;
Figure 10 is a perspective view of the inductive element shown in Figure 9;
Figure 11 is a top plan view of layer one in the embodiment shown in Figure 9;
Figure 12 is top plan view of layer two in the embodiment shown in Figure 9;
Figure 13 is a top plan view of layer three in the embodiment shown in Figure 9;
Figure 14 is a front elevational view of the combined effect of the layers one through three in forming an inductive element;
Figure 15 is an enlarged top plan view of the substrate under an integrated inductor in accordance with one embodiment of the present invention;
Figure 15a is an enlarged top plan view of the substrate under an integrated inductor in accordance with one embodiment of the present invention; and
Figure 16 is an enlarged cross-sectional view taken generally along the line 16-16 in Figure 15.

Detailed Description

[0012] Referring to Figure 1, an integrated circuit 10 may include analog circuit elements operating above 100 megahertz, such as RF components 12, mixed signal components 14 and logic and memory components 16, all integrated within the same monolithic integrated circuit. Coupling between the radio frequency circuit elements, such as inductors, capacitors and transistors and the substrate on which the components are all integrated can be reduced, if not effectively eliminated, by creating an effective reverse biased diode between the radio frequency component and the substrate. This reverse biased diode may be formed using a triple well fabrication process in which the inductive circuit element is formed over a triple well.

[0013] In addition, memory components such as flash memory and static random access memory (SRAM) may be made on the same process, in the same substrate, utilized to form logic circuits such as microprocessors and digital signal processors. For example, the processes disclosed in U.S. Patents 5,926,418 and 5,867,425, assigned to the assignee of the present application, may be utilized to form both logic devices and flash memory.

[0014] A radio frequency transceiver useful in a cellular telephone 10a, shown in Figure 2, includes an antenna 18, a radio frequency section 20, a logic section 22, a memory 26 and an interface 24. The interface 24 provides the graphical user interfaces that may be displayed on display screens to implement the functions of the cellular telephone 10a. The logic circuit 22 may also include a microprocessor which operates using a memory 26. In one embodiment of the present invention, the memory 26 is a flash memory. The radio frequency section 20 may include a number of passive components including inductive circuits.

[0015] The radio frequency section 20 as well as the antenna 18 may be formed using integrated circuit techniques to create a single integrated circuit that includes all of the components 18, 20, 22, 24 and 26, in accordance with one embodiment of the present invention. In other embodiments, some but not all of the analog and digital components may be fabricated on the same integrated circuit chip.

[0016] Generally, complementary metal oxide semiconductor techniques may be utilized to form all of the components depicted in Figure 2 on a single chip. However, in some cases, particular components may be split among two or more integrated circuits. However, the designer is free to position particular components on particular integrated circuits based on design considerations rather than process and technology incompatibilities. Again, the problem of coupling of unwanted signals to the RF components included in the radio frequency section 20 may be avoided by forming an effective reverse biased diode in the common substrate utilized to form all the components of the telephone 10a.

[0017] Similarly, an integrated transceiver 10b for a wireless network, for example in accordance with the Bluetooth specification may be fabricated using the same principles. The Bluetooth transceiver 10b includes an antenna 28 coupled to a radio 30. The radio 30 is coupled to a link baseband controller or link controller 32. A central processor unit 34 couples an interface 36 and a memory 38. In some embodiments of the present invention, the memory 38 may be a flash memory. All of the components may be integrated into a single chip in one embodiment.

[0018] An integrated radio frequency (RF) element 40 that may be utilized in connection with the RF section 20 or the radio 30 of the embodiments of Figures 2 and 3 or any other integrated circuit using an inductive element, is shown in Figure 4. In this case, a triple well is defined within the substrate 42 by a P-well 46, a deep N-well 44 and the P-type substrate 42. The P-well 46 is a well or tub within the deep N-well 44.

[0019] Two reverse biased pn junctions are created, one by the juxtaposition of the P-well 46 and N-well 44, and another by the juxtaposition of the P-type substrate 42 and the N-well 44. Both pn junctions may be biased

by a potential V_B on the N-well 44. For example, if the P-well 46 and P-type substrate 42 are grounded, increasing the bias potential on the N-well 44 increases the bias on each junction. In some embodiments, if the N-well 44 is biased, the P-well 46 floats.

[0020] Depletion regions are formed by the junction bias, adding a depletion capacitance across the pn junctions between the P-well 46 and N-well 44 and between the N-well 44 and the P-type substrate 42. These depletion capacitances can be reduced by increasing the bias across the pn junctions. The higher the junction bias, the more reduction in the junction capacitance, reducing the total capacitance. Reducing total capacitance reduces the capacitive coupling of the RF circuits to the substrate and the self-resonance frequency of the inductive element 40. The reverse biased junctions reduce the coupling of noise or other unwanted signals between the substrate 42 and the RF integrated circuit components, formed over the substrate 42, such as the capacitor 48 or the inductive element 50.

[0021] The layer 54 is conventionally formed of an oxide. Of course, the present invention is equally applicable to multi-layer metal processes in which the passive components, such as the inductive element 50, are formed in any desired metal layer.

[0022] The techniques for forming triple wells are well known. For example, U.S. Patents 5,926,418 and 5,867,425 (assigned to the assignee of the present application) provide an explanation of exemplary processes for forming a triple well. The triple well process is equally applicable to manufacturing flash memory devices. By using the triple well process, a flash memory may be formed in the same integrated circuit with logic family components such as processors and digital signal processors.

[0023] Referring next to Figure 5, the inductive element 50 may be formed of a planar, spiral-shaped layer defined over the substrate 42, for example atop a oxide layer 54. Conventionally, the inductive element 50 is formed by patterning and deposition techniques. However, any technique for forming the inductive element 50 may be utilized. The resulting structure may be formed of a spiral-shaped flat ribbon that may include a plurality of interconnected straight sections such as the sections 58a and 58b. Advantageously, the element 50 is positioned over the P-well 46 of the triple well 40. Appropriate electrical connections may be made through various layers to electrically couple the ends of the inductive element 50 to the rest of the integrated circuit.

[0024] Alternatively a non-planar design may be used as shown in Figure 7 and as described, for example in U.S. Patent 5,545,916 to Koullias. The spiral inductive element 50, shown in Figure 5, may have a non-planar cross-section as indicated in Figure 7 including a rectangular portion 70 and a circular portion 72. Each of the trace elements 58c and 58d are arranged such that the material thickness favors the innermost edge "O". Thus, the trace shown in Figure 7 is from the left side of the spiral inductive element 50 (shown in Figure 5). The material is added close to an edge "O" where the current may flow at higher frequencies.

[0025] As another alternative, the spiral inductive element 50 may have an non-rectangular configuration such as the multilevel, multi-element polygonal design, for example, as set forth in U.S. Patent 5,559,360, and as shown in Figure 8. Referring to Figure 8A, the layer with wires A_1 through A_{10} has a first end A that is designated by the connective structure CON1. A group often connective wires, A_1, A_2, A_{10}, are shown in the center of the spiral. The wires B_1-B_{10} of the second layer, shown in Figure 8B, are centrally connected to the wires A_1 through A_{10} inverse sequentially. The output of the spiral inductive element is identified as a parallel connection CON2 in Figure 8B that forms the parallel connections of all the elements of the B level. Through the use of multiple parallel conductive elements arranged on the substrate (in lieu of a single element conductive path), the resistance may be decreased and self-inductance increases. The decreased resistance and increased inductance may result in an improved quality factor (Q).

[0026] A multi-layer non-planar integrated inductor design, as shown in Figures 9 through 14, may also be used as the inductive element 50 (Figure 5), as described in U.S. Patent 6,008,102. A series of three conductive layers one, two and three, are progressively coated one on top of another as shown in Figure 9. The three layers combine to form an integrated helical coil as shown in Figure 14. The first layer is formed of a conductive material in the shape shown in Figure 11, the second layer is formed of a conductive material in the shape shown in Figure 12 and the third layer is formed of conductive in the shape shown in Figure 13. The net effect of the three layers is the coil shown in Figure 14. The angular coil 450, shown in Figure 10, has a series of multiple loops that are set perpendicularly to the plane of the substrate.

[0027] Referring again to Figure 9, a layer 304 is coated over a passivated wafer. The layer 304 may be formed of a conductive material such as titanium-tungsten (TiW) to form a barrier layer and provide for the adhesion of a subsequently sputtered layer of copper 306. An initial photoresist layer 406 and a second photoresist 408 define the intervening conductive material. The layer 414 may be a sputtered conductor, and a layer 420 is a third layer of plated metal while the material 416 may be photoresist.

[0028] An equivalent circuit, shown in Figure 6, for the inductive element 50 (Figure 5) includes an inductance 62a which may arise from all or any part of the spiral-shaped inductive element 50. The inductive element 50 may also be represented by resistance 62b which arises from the natural resistance of the material utilized to form the spiral-shaped inductive element 50. A capacitance 64 arises from the capacitance between the inductive element 50 (or any other RF component such

as transistors and capacitors) and the substrate 42 and particularly by the intervening dielectric layer 54. An additional resistance 66a may arise from the material utilized to form the P-well 46.

[0029] The effect of the pn junction created by the P-well 46 and the N-well 44 is represented by the diode 66b and the effect of the pn junction created by the N-well 44 and P-type substrate 42 is represented by the diode 66c. The capacitance 67b and the diode 66c reduce the coupling from the substrate 42 back to the inductor 50.

[0030] The reverse biased diode 66b, oriented oppositely to the diode 66c, reduces the inductive element 50 capacitive coupling losses to the substrate 42. Through the creation of the diode 66c, an effectively infinite resistance is created to reduce interference by substrate signals with the element 50 (and any other RF circuits). In particular, the inductive element 50 may be a highly tuned element that may be adversely affected by noise and other unwanted signals present in the substrate 42. These signals may be present in the substrate 42 due to the formation of a wide variety of other circuit elements in the same integrated circuit. These unwanted signals are isolated from the sensitive inductive element 50 by the reverse biased diode 66c.

[0031] As a result, a variety of different circuit types, including radio frequency circuit elements, mixed signal circuit elements, logic elements and memory elements, including flash memory elements, may all be formed in the same integrated circuit in the same substrate 42. Therefore, greater integration is possible and more efficient and lower cost radio frequency devices, such as Bluetooth transceivers and cellular telephones wireless local area networks, may be fabricated.

[0032] The benefits of the triple well can be further appreciated by comparing a triple well approach to a approach in which a single well such as a deep N-well is utilized below the inductive element 50. The impedance caused by the deep N-well, in a deep N-well embodiment, may be represented by the value R_w. The total impedance, R, from the inductive element 50 to the substrate then may be represented by the equation:

$$\frac{1}{R}=\frac{1}{R_w}+j\omega C_w$$

where C is the capacitance resulting from the oxide between the inductive element 50 and the substrate and the capacitance of the substrate and ω is the frequency. Similarly, the total capacitance, C_w, for the series, is expressed as follows:

$$\frac{1}{C_w}=\frac{1}{C_{OX}}+\frac{1}{C_{SUB}}$$

where C_{OX} is the capacitance due to the dielectric between the inductive element 50 and the substrate and C_{SUB} is the capacitance between the inductive element 50 and the substrate.

[0033] In contrast the total impedance, R_T, of the triple well is expressed as (indicated as 64 follows:

$$\frac{1}{R_T}=\frac{1}{R_j}+j\omega C_T$$

where R_j is the resistance 66a of the N-well and C_T is the capacitance of the triple well (indicated as 64 in Figure 6).

[0034] Similarly, the series capacitance created by the triple well, C_T, is as follows:

$$\frac{1}{C_T}=\frac{1}{C_{ox}}+\frac{1}{C_j}+\frac{1}{C_{SUB}}$$

where C_{ox} is the capacitance 64 due to the oxide between the inductive element 50 and the substrate, C_j is the capacitance 67a arising from the junction between the P-well and the N-well and C_{SUB} is the capacitance 67b between the N-well and the substrate.

[0035] Since the impedance arising from the junction R_j is much greater than the impedance without the junction, the effect of the triple well is to substantially increase the impedance compared to a single deep N-well. Moreover, the capacitance created by the triple well can be adjusted by the N-well bias to be less than the capacitance created by the deep N-well. Thus, the coupling that results from the capacitance in the triple well is significantly less. Since the total impedance of the triple well is much greater than the impedance of the deep N-well and the capacitance of the triple well is less, there is less capacitive and resistive coupling to the substrate and also better noise isolation from the substrate to the RF circuits arising from the use of the triple well compared to the use of only a deep N-well.

[0036] The self-resonance frequency may also be improved in some embodiments, by reducing the total capacitance. The self-resonance frequency is proportional to $1/(LC)^{1/2}$, so that the lower the capacitance, the higher the self-resonance frequency or the better the high frequency performance of the inductor 50. Reducing the capacitive coupling also improves the quality factor or Q of the inductor 50.

[0037] While an illustrated embodiment using a triple well is described, additional wells may be incorporated to form a series of one or more additional diodes in other embodiments.

[0038] Even in integrated inductors with dramatically decreased capacitive coupling, magnetic coupling may still be a problem. Magnetic coupling may be a problem in at least two regards. Firstly, magnetic coupling may adversely affect the operation of an integrated inductor when other inductors are integrated within the same

substrate. In addition, the magnetic coupling may adversely affect the power consumption of integrated circuits that include at least one integrated inductor. Magnetic coupling may cause eddy currents in the substrate.

[0039] Referring to Figure 15, an integrated inductor 40a may include a P-type substrate 42 with a deep N-well 44 formed therein. A P-well 46a may be formed within the deep N-well 44. A trench 80 may be defined in the substrate 42 extending completely across the P-well 46a. In one embodiment of the present invention, the trench structure 80 is in a plurality of arms extending from the center for example in an X-shape. Figure 15a shows another embodiment with three equally spaced arms 79 forming a trench 80a. Advantageously, the trench structure 80 radiates outwardly from the center of the P-well 46a in the form of three or more arms.

[0040] The trench structure 80 may be formed using conventional trench techniques widely utilized in connection with CMOS integrated circuit fabrication processes. The trench structure 80 may extend completely across the P-well 46a in two dimensions.

[0041] Referring to Figure 16, the trench structure 80 may extend into the P-well 46a to a depth of approximately .4 to .5 microns in one embodiment of the present invention. Advantageously, the trench structure 80 extends deep enough into the P-well 46a to disrupt and push the space (image) eddy currents (arising from magnetic coupling) deeper into the substrate. By providing a gridwork of trench structures 80, the loss from the image eddy currents may be effectively reduced in one embodiment of the invention.

[0042] The trench structure 80 is advantageously filled with an insulator, such as oxide, in one embodiment of the present invention. Forming trenches and filling the trenches with insulators are well understood by those skilled in the art of CMOS process design.

[0043] While the present invention has been described with respect to a limited number of embodiments, those skilled in the art will appreciate numerous modifications and variations therefrom. It is intended that the appended claims cover all such modifications and variations as fall within the true spirit and scope of this present invention.

Claims

1. An integrated circuit comprising:

   a substrate;
   a spiral inductive element formed over said substrate; and
   a trench formed in said substrate beneath said inductive element.

2. The circuit of claim 1 wherein said circuit is a complementary metal oxide semiconductor circuit

3. The circuit of claim 3 wherein said trench is formed in a x-shape.

4. The circuit of claim 3 wherein said trench includes a plurality of arms which radiate outwardly from a center.

5. The circuit of claim 4 including at least three arms.

6. The circuit of claim 1 including a triple well formed in said substrate, under said inductive element.

7. The circuit of claim 6 wherein said triple well includes an N-well with a P-well formed in said N-well and wherein said substrate is a P-type substrate.

8. The circuit of claim 7 wherein said N-well is a deep N-well.

9. The circuit of claim 8 wherein said inductive element is formed over said P-well.

10. The circuit of claim 9 wherein said trench extends completely across said P-well.

11. The circuit of claim 1 including a memory formed in said substrate.

12. The circuit of claim 11 wherein said memory is flash memory.

13. The circuit of claim 1 wherein said circuit is a radio frequency device.

14. The circuit of claim 13 wherein said radio frequency device is a cellular telephone.

15. The circuit of claim 1 wherein said circuit is a wireless network transceiver.

16. The circuit of claim 15 wherein said circuit is a Bluetooth transceiver.

17. The circuit of claim 1 including logic circuits formed in said substrate.

18. The circuit of claim 17 including memory formed with logic circuits in said substrate.

19. The circuit of claim 6 wherein said triple well forms a reverse biased diode between the substrate and said inductive element.

20. A method comprising:

    forming an inductive element over a substrate; and
    forming a trench in said substrate beneath said

inductive element.

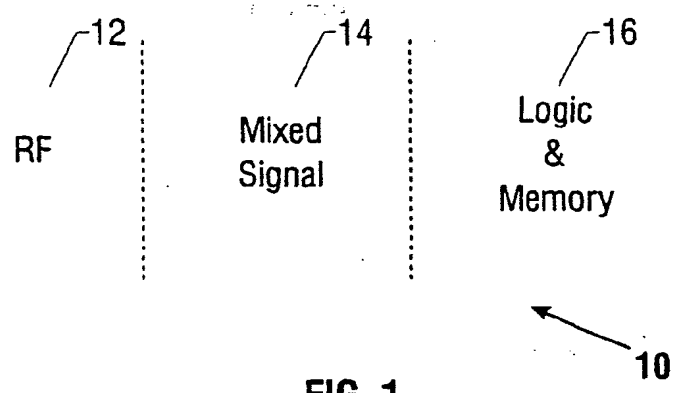

FIG. 1

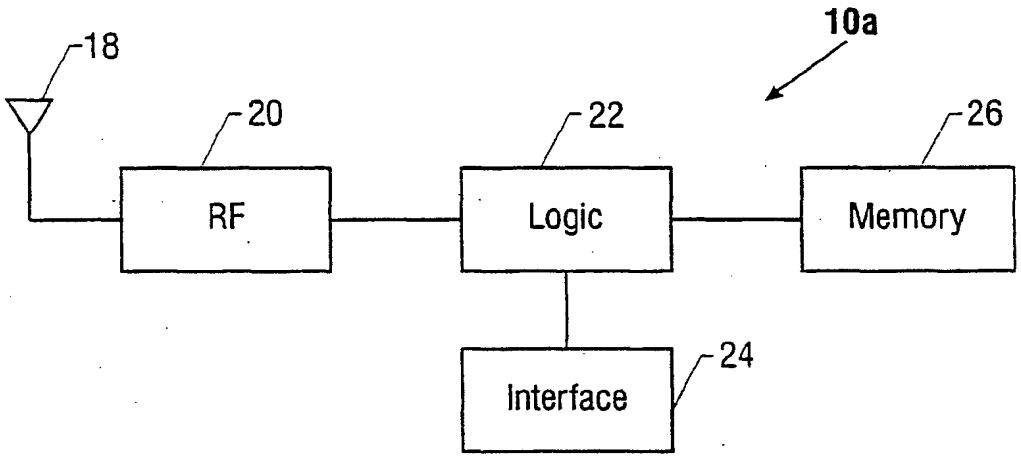

FIG. 2

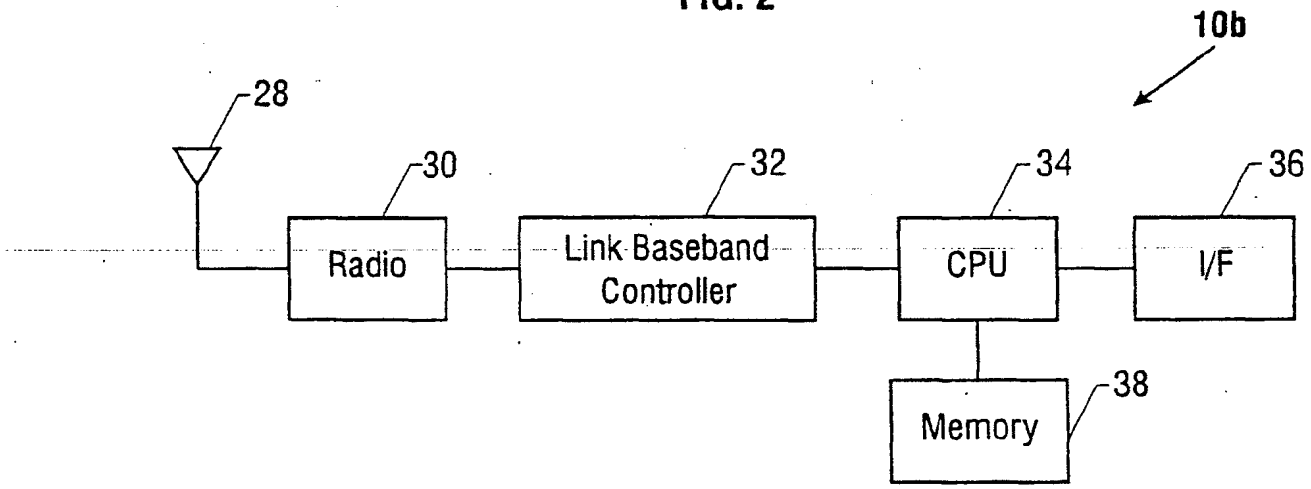

FIG. 3

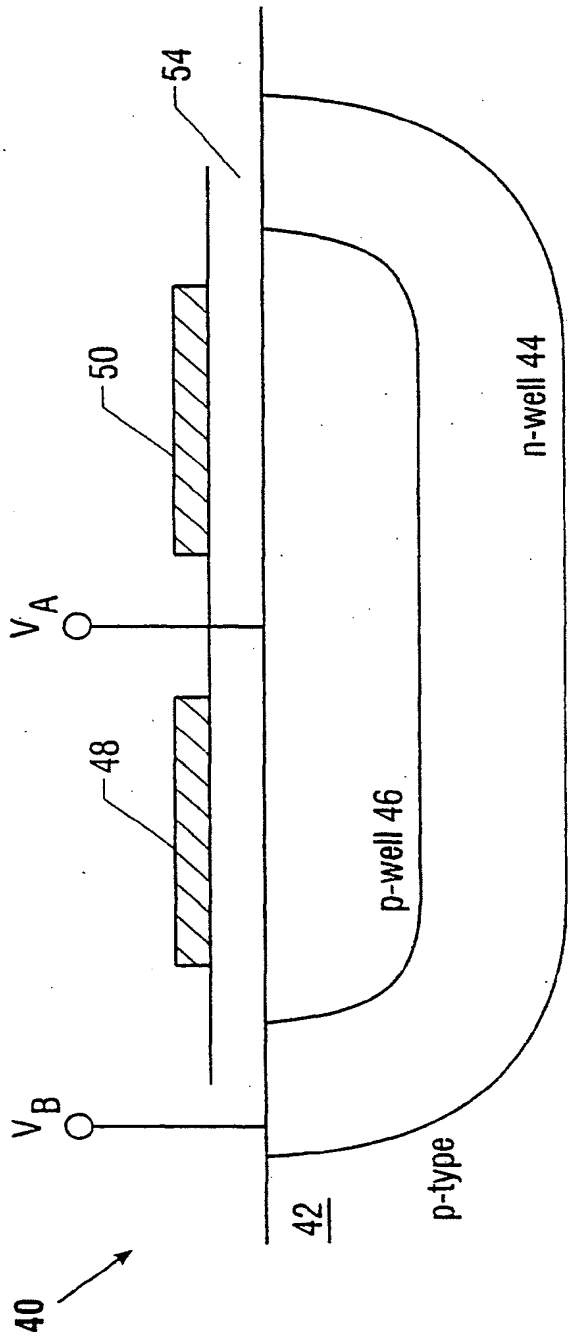

FIG. 4

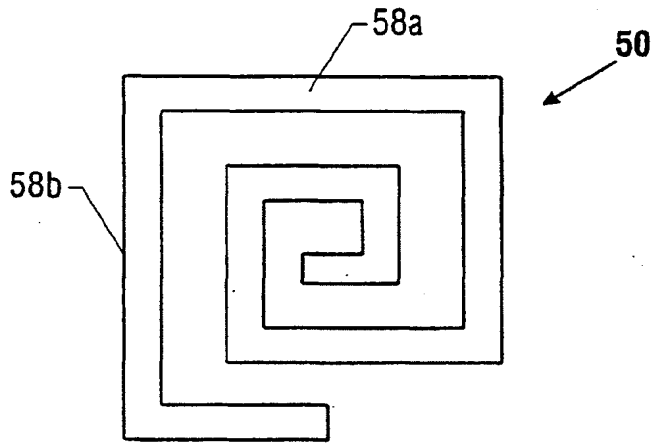

FIG. 5

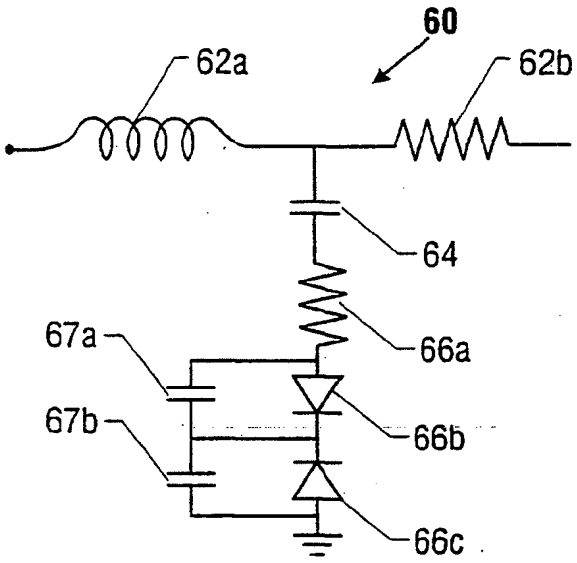

FIG. 6

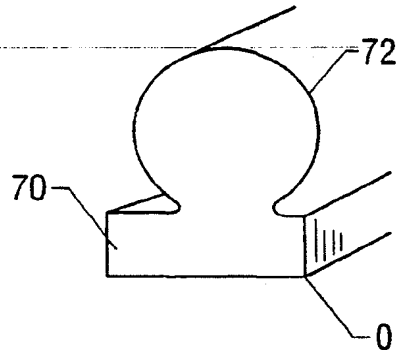

FIG. 7

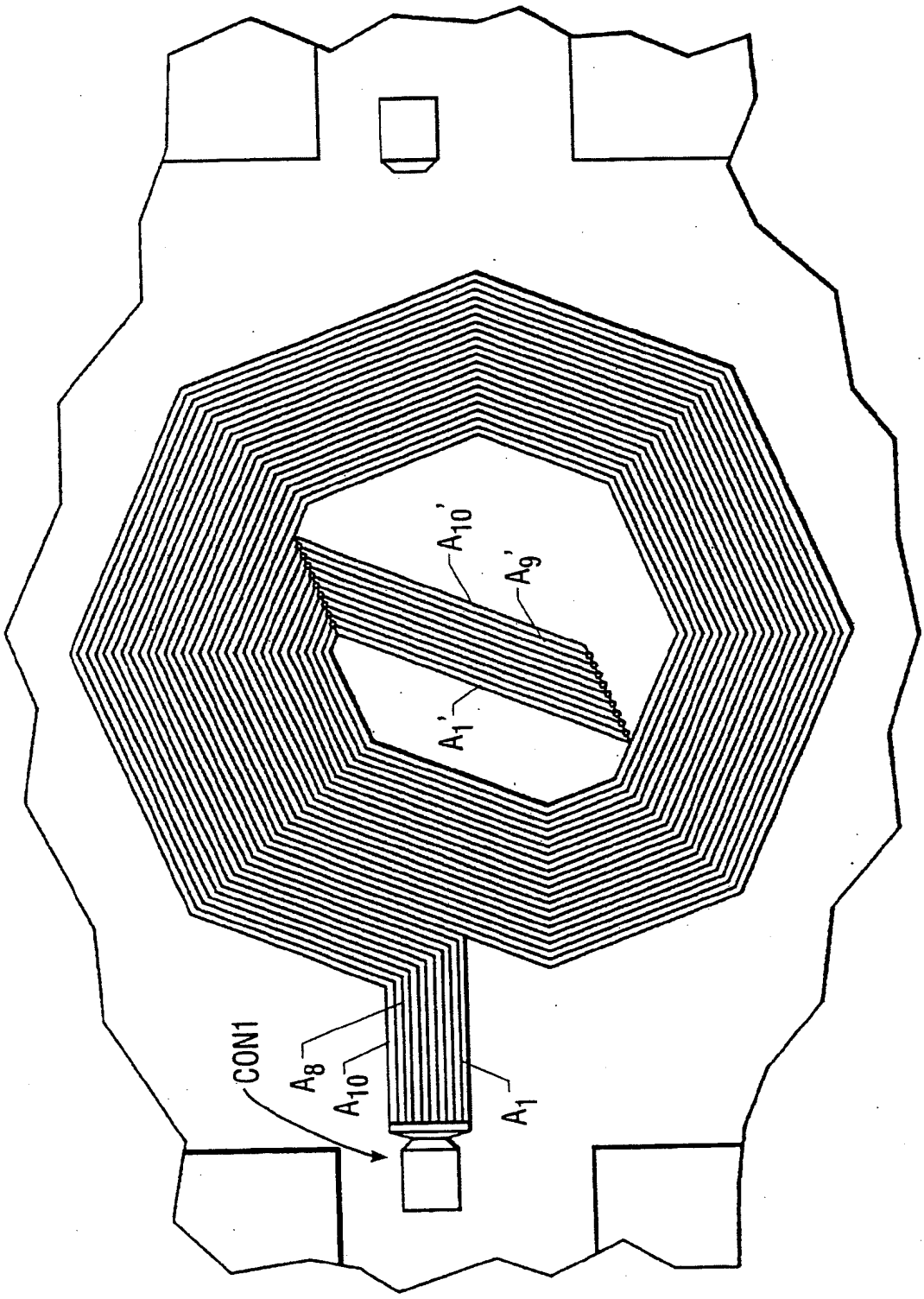

FIG. 8A

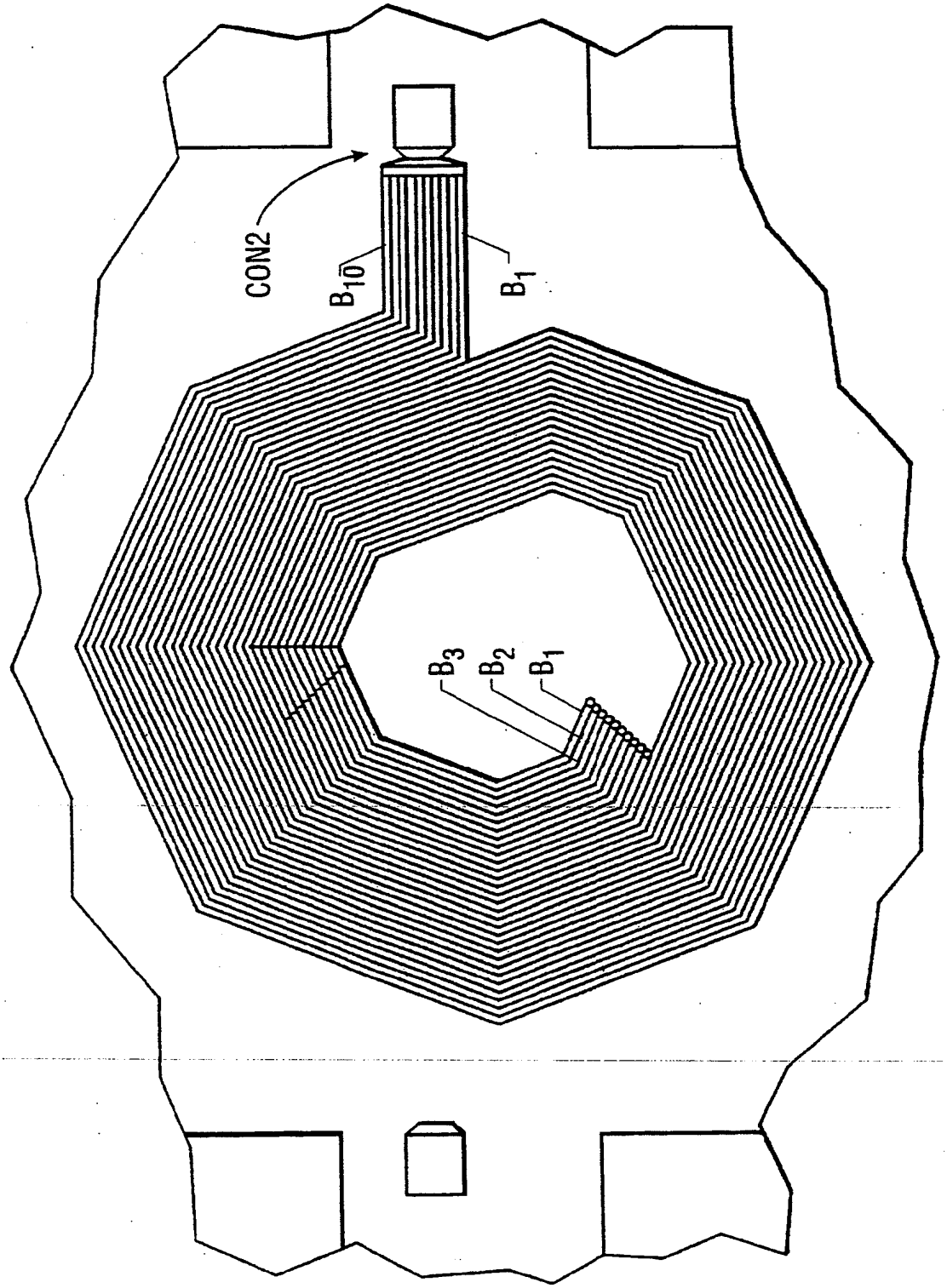

FIG. 8B

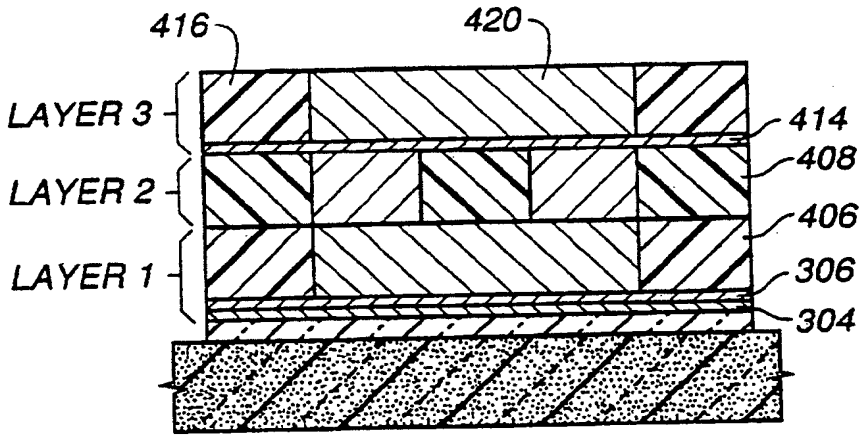

FIG. 9

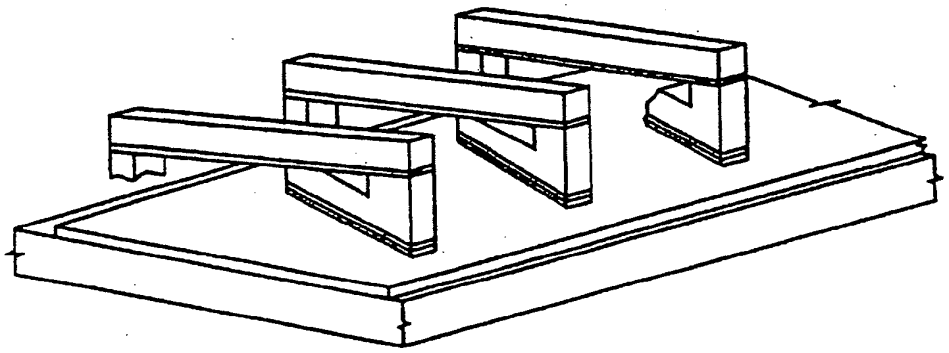

FIG. 10

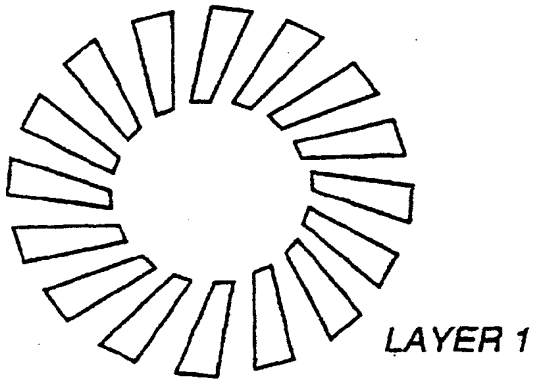

FIG. 11

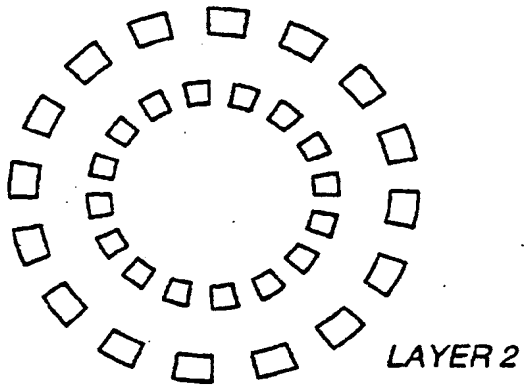

FIG. 12

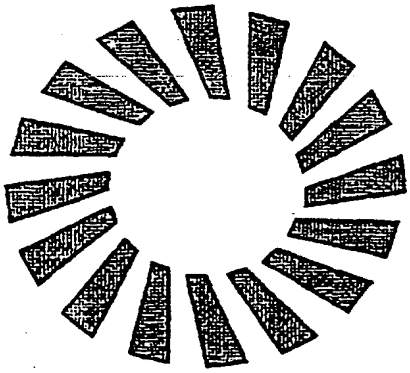

FIG. 13

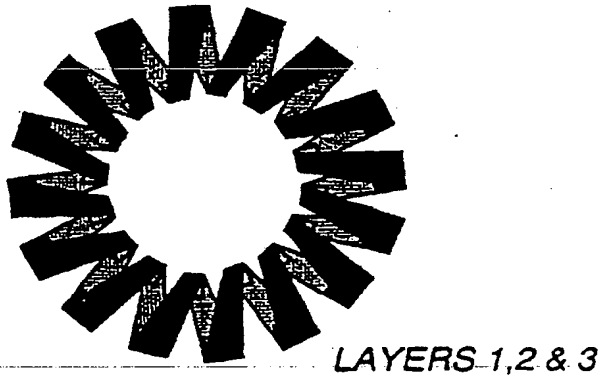

FIG. 14

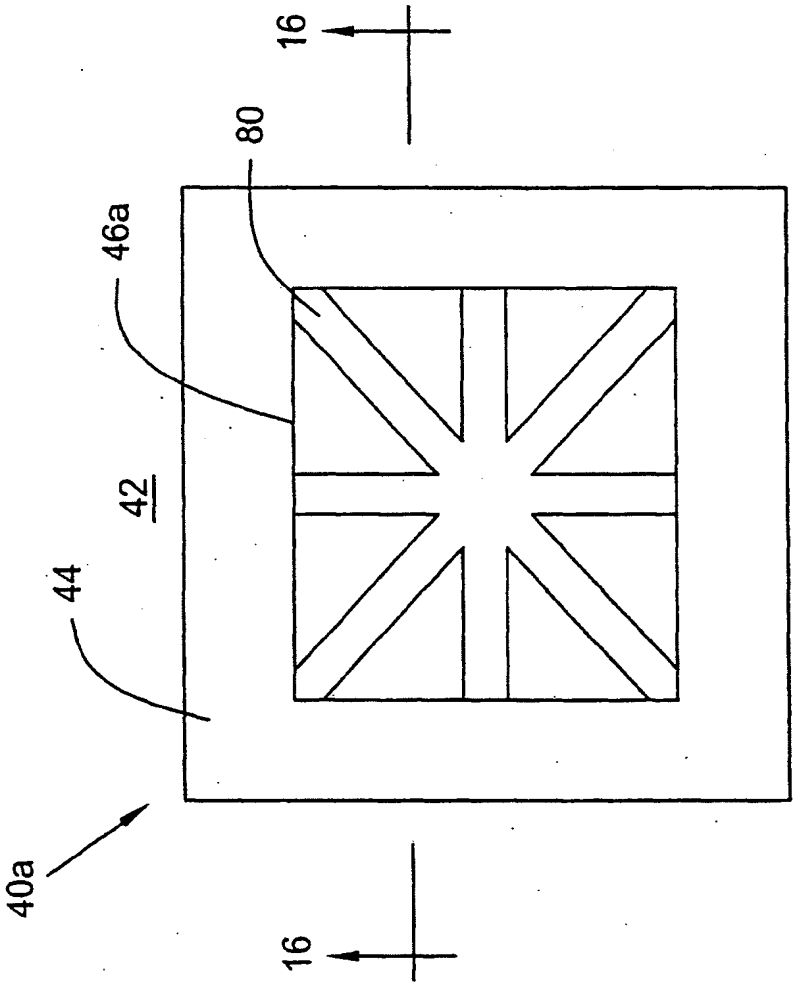

FIG. 15

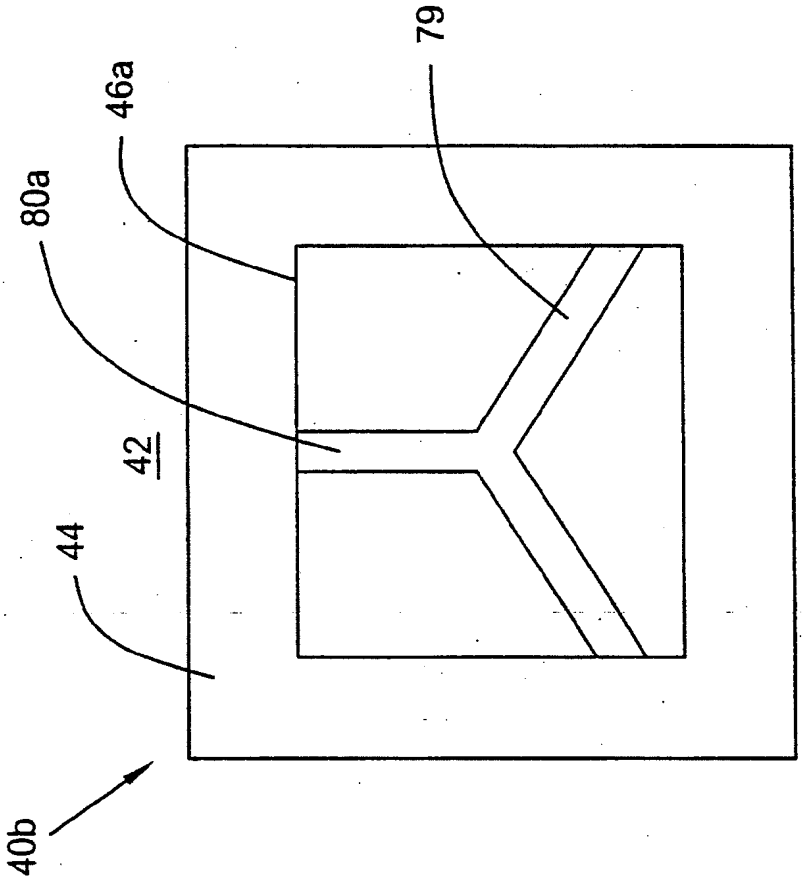

FIG. 15a

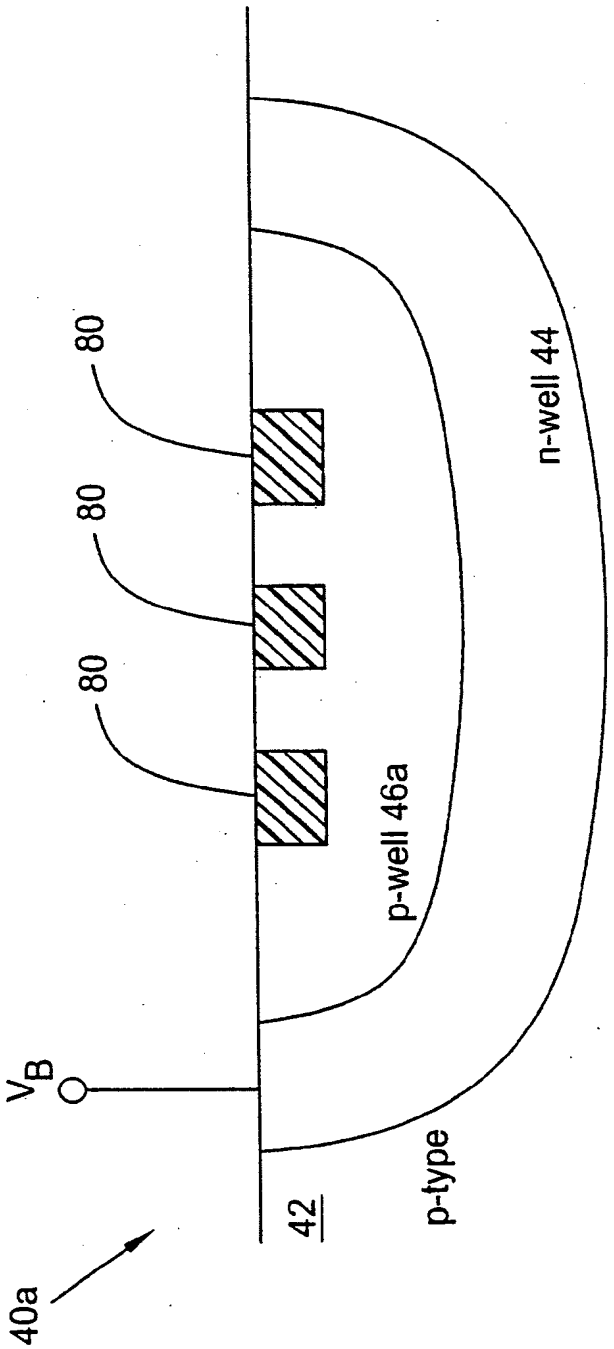

FIG. 16

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(54) Integrated inductive circuits

(57) An integrated inductive element (40a) may be formed over a substrate (42). A trench (80) may be defined in a variety of shapes in the substrate (42) beneath the integrated inductive element (40a) in order to reduce eddy current losses arising from magnetic coupling between integrated inductors associated with the same integrated circuit.

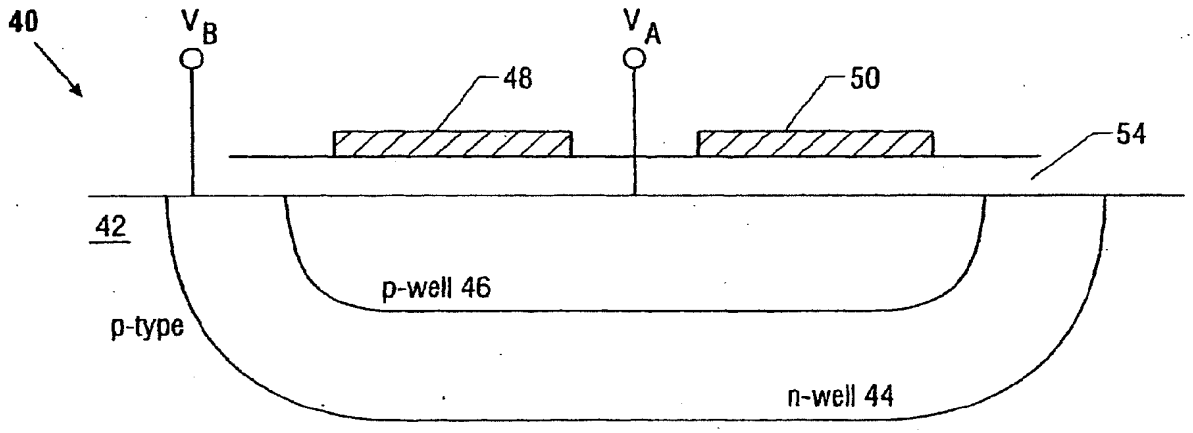

FIG. 4

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EUROPEAN SEARCH REPORT

Application Number
EP 01 20 1775

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The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
THE HAGUE	8 July 2003	Wirner, C

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